instruction fetching means that are connected to said bus to fetch instruction groups via said bus from said memory, certain of said instruction groups including at least one instruction that, when executed, causes an access to an operand or an instruction [accesses operands or instructions] or both, said [operands] operand [and instructions] or instruction being located relative to a boundary of said instruction groups;

an instruction register for receiving a first of said instruction groups from said instruction fetching means, said first of said instruction groups including [one or more operands] an operand or at least two sequential instructions or both;

instruction supplying means for supplying, in succession from said instruction register, said [one or more] operand or sequential instructions of said first of said instruction groups to said central processing unit;

instruction decoding means for configuring said instruction supplying means to select from said instruction register an operand associated with one of said instructions from said first of said instruction groups.

~~72~~(Three Times Amended). The microprocessor system of claim ~~71~~ wherein said instruction decoding means further includes means, responsive to a SKIP instruction in said instruction register, for configuring said instruction fetching means such that the next instruction group is supplied to the instruction register, and for configuring said instruction supplying means to supply in succession from said instruction register, said [one or more] sequential instructions, beginning with the first instruction in said instruction register from said next instruction group, to said central processing unit.

~~73~~(Three Times Amended). The microprocessor system of claim ~~72~~ further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said SKIP instruction and said predefined condition to execute or not execute said SKIP instruction based on existence of said predefined condition.

74(Three Times Amended). The microprocessor system of claim 71 further comprising:

a loop counter that is connected to receive a decrement control signal from said instruction decoding means, said instruction decoding means further including means, responsive to a MICROLOOP instruction in said instruction register, configured to supply said decrement control signal to said loop counter, said instruction supplying means being configured to supply from said instruction register said [one or more] sequential instructions, beginning with the first instruction in said instruction register, from said first of said instruction groups, to said central processing unit.

75(Twice Amended). The microprocessor system of claim 74 further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said MICROLOOP instruction and said predefined condition to execute or not execute said MICROLOOP instruction based on existence of said predefined condition.

78(Three Times Amended). The microprocessor system of claim 71 wherein said instruction decoding means configures said instruction supplying means to supply to said central processing unit a last byte of said first of said instruction groups as said operand in response to one of said [one or more] sequential instructions within said first of said instruction groups.

79(Twice Amended). The microprocessor system of claim 71 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said [one or more] sequential instructions within said first of said instruction groups.

80(Twice Amended) The microprocessor system of claim 71 wherein said instruction decoding means are configured to supply control signals to said

instruction fetching means such that a subsequent one of said instruction groups supplied to said instruction register is determined in response to a branch-type instruction in said [one or more] sequential instructions within said first of said instruction groups.

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81(Twice Amended). The microprocessor system of claim 77 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups supplied to said instruction register is determined in response to a branch-type instruction in said [one or more] sequential instructions within said first of said instruction groups.

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82(Twice Amended). The microprocessor system of claim 80 further comprising a counter connected to said instruction supplying means, said counter providing a count signal indicative of an instruction of said subsequent one of said instruction groups that is to be provided to said central processing unit by said instruction supplying means, said counter being reset in response to receipt by said instruction decoding means of said branch-type instruction in said [one or more] sequential instructions.

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83(Twice Amended). The microprocessor system of claim 80 further comprising means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said branch-type instruction and said predefined condition to execute or not execute said branch-type instruction based on existence of said predefined condition.

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84(Twice Amended). The microprocessor system of claim 71 wherein said instruction fetching means fetches said [one or more] sequential instructions in parallel for each of said instruction groups in a single memory cycle.

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85(Twice Amended). The microprocessor system of claim 71 further comprising:

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memory access testing means for testing said first of said instruction groups to determine if said [one or more] sequential instructions require a memory access; and

if said memory access testing means determine a memory access is not required, then supplying of control signals to said instruction fetching means to fetch the next instruction group during the execution of a current of said instruction groups.

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~~91~~(Twice Amended). A microprocessor comprising:

a central processing unit;

an instruction register operatively coupled to said central processing unit;

instruction fetching means for providing instruction groups to said instruction register wherein certain of said instruction groups include [one or more operands] an operand or at least two sequential instructions or both; said [one or more] operand or sequential instructions including at least one instruction that, when executed, causes an access to an operand or an instruction [accesses operands or instructions] or both , said [operands] operand or [and instructions] instruction being located relative to a boundary of said instruction groups;

instruction supplying means for successively coupling said [one or more] operand or sequential instructions of said certain of said instruction groups to said central processing unit; and

instruction decoding means for configuring said instruction supplying means to select operands from said instruction register associated with particular ones of said sequential instructions.

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~~92~~(Twice Amended). The microprocessor of claim ~~91~~ wherein said instruction decoding means, upon receiving a SKIP one of said [one or more] sequential instructions from a current one of said instruction groups, configures said instruction fetching means to fetch a next one of said instruction groups to said instruction register, and configures said instruction supplying means to supply a first [of] one of said [one or more] sequential instructions.

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~~93~~(Twice Amended). The microprocessor of claim ~~92~~ further including means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said SKIP instruction and said predefined condition to execute or not execute said SKIP instruction based on existence of said predefined condition.

Sub 76 23 20
~~94~~(Twice Amended). The microprocessor of claim ~~91~~ further comprising a loop counter, said instruction decoding means, responsive to a MICROLOOP instruction within said instruction register, providing a decrement signal to said loop counter, and said instruction supplying means being configured to supply from said instruction register said [one or more] sequential instructions, beginning with the first instruction in said instruction register, from a current one of said instruction groups, to said central processing unit.

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~~95~~(Amended). The microprocessor of claim ~~94~~ further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said MICROLOOP instruction and said predefined condition to execute or not execute said MICROLOOP instruction based on existence of said predefined condition.

Sub 77 29
~~97~~(Twice Amended). In a microprocessor system including a central processing unit, memory and an instruction register, a method for providing instructions from said instruction register to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include [one or more operands] an operand or at least two sequential instructions or both, said [operands and] operand or instructions being located relative to a boundary of said instruction groups;

supplying, in succession from said instruction register, said [one or more] operand or sequential instructions of said certain of said instruction groups to said central processing unit; and

selecting an operand from said one of said instruction groups for use by said central processing unit.

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~~98~~(Amended). The microprocessor of claim ~~96~~ wherein said instruction decoding means includes means for configuring said instruction supplying means to supply a remainder of a current one of said instruction groups within said instruction register as [one of] said [operands] operand to said central processing unit.

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~~99~~(Twice Amended). The microprocessor of claim ~~91~~ wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said [one or more] sequential instructions.

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~~100~~(Twice Amended). The microprocessor of claim ~~96~~ further comprising means for determining whether a predefined condition exists within said microprocessor system, and means for controlling response of said instruction decoding means to branch-type ones of said instructions and said predefined condition to execute or not execute said branch-type ones of said instructions based on existence of said predefined condition.